5 - 18GHz Surface Mount Amplifier with Integrated Bias

Features

- Wide operating range: 5-18GHz
- 3.3V, 100mA drain bias (gate N/C) for gain and NF:
  - 13 ±0.4dB gain, 7dB NF, 16dBm Psat, 13.5dBm P1dB
- 5V, 130mA drain bias (gate N/C) for power:
  - 12.5 ±0.7dB gain, 9dB NF, 19.5dBm Psat, 17dBm P1dB
- Single supply voltage with self-biasing gate OR direct control of both gate and drain stages

Application

The UA5M15MP is ideally suited for:

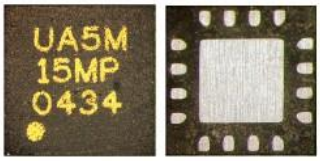
- Point-to-point and point-to-multipoint digital radio
- Spread spectrum broadband communications
- LO driver or mixer isolation amplifier
- General isolation and gain block amplifier

Description

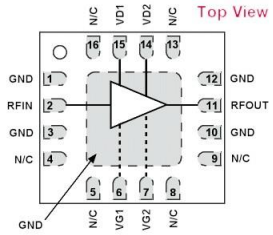
The UA5M15MP is a two-stage pHEMT amplifier MMIC in a Pb-free leadless plastic QFN package. The IC features a positive gain slope that offsets package loss, resulting in a SMT part with excellent gain flatness across a broad bandwidth. The device can be operated at 5V 130mA for power applications, or 3.3V 100mA for low-noise and gain.

Surface Mount Package

- 16-pin Pb-free SMT QFN package
- 3x3mm pkg size; 0.5mm pad pitch



Functional Diagram

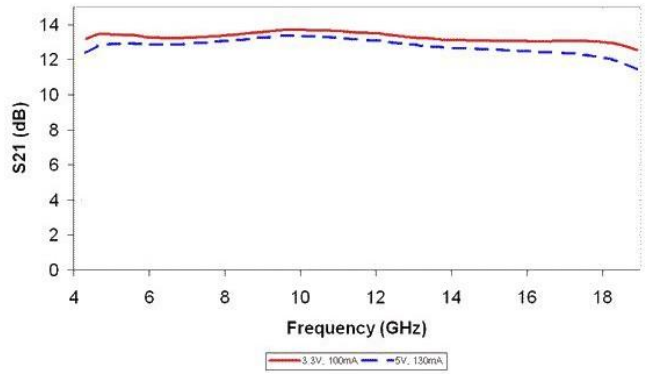


Key Characteristics: Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C Vd=Vd1=Vd2, Vg=Vg1=Vg2, Id=Id1+Id2, Zo=50Ω

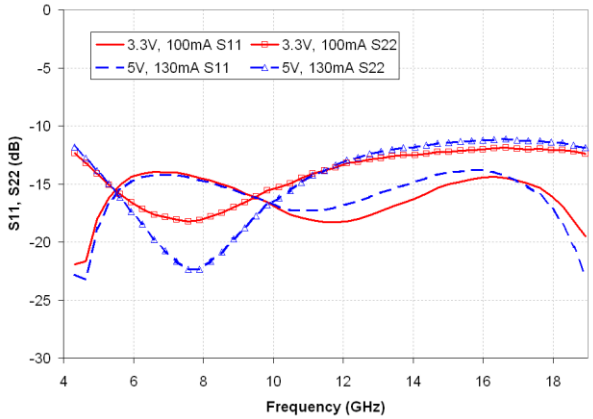
	Frequency Range: 5 - 18GHz	Gain Bias: Vd=3.3V, Vg=N/C, Id=100mA			Power Bias: Vd=5V Vg=N/C, Id=130mA		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
S21 (dB)	Small Signal Gain	-	13	-	-	12.5	-
Flatness (±dB)	Gain Flatness	-	0.4	-	-	0.7	-
S11 (dB)	Input Match	-	-14	-	-	-14	-
S22 (dB)	Output Match	-	-11	-	-	-11	-
S12 (dB)	Reverse Isolation	-	-35	-	-	-35	-
P1dB (dBm)	1dB Compressed Output Power	-	13.5	-	-	17	-
Psat (dBm)	Saturated Output Power	-	16	-	-	19.5	-
NF (dB)	Noise Figure	-	7	-	-	9	-

Typical Probed Performance QFN Package

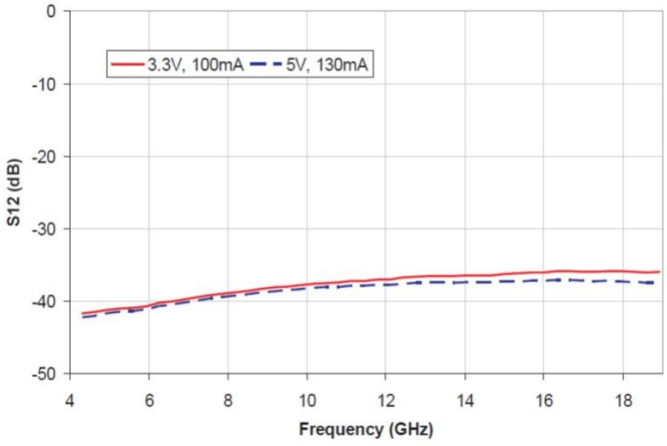
S21



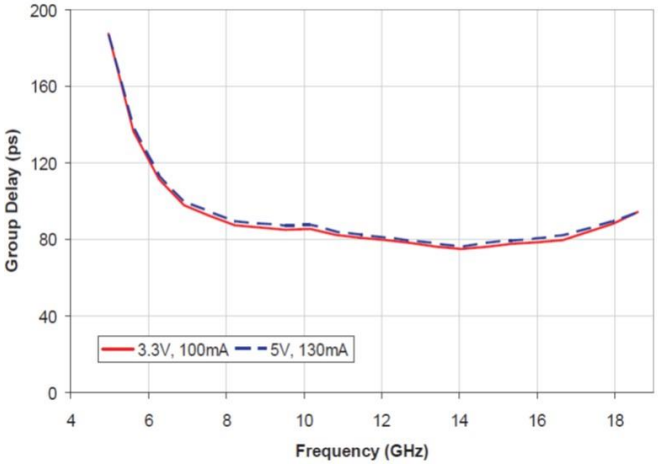
S11, S22



S12

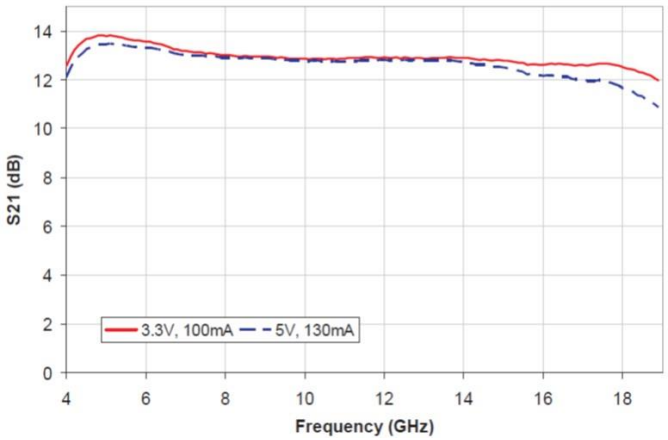


Group Delay

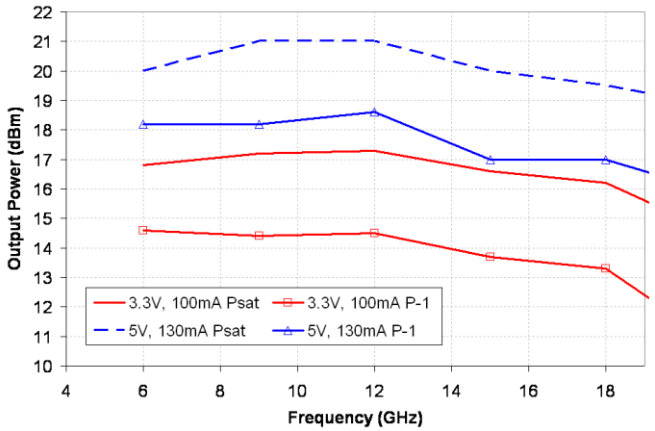


Supplemental Tested in Evaluation Fixture

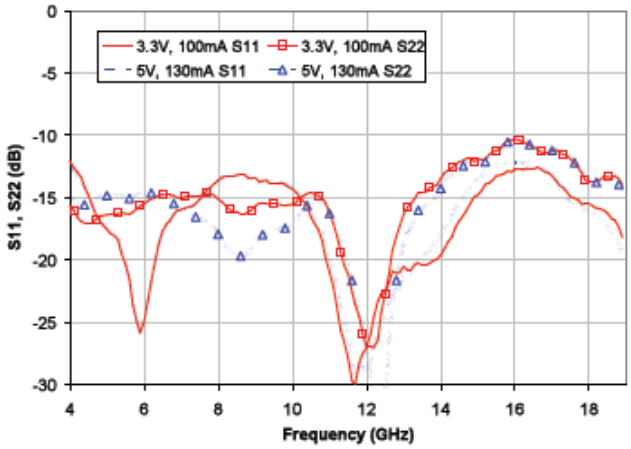
S21



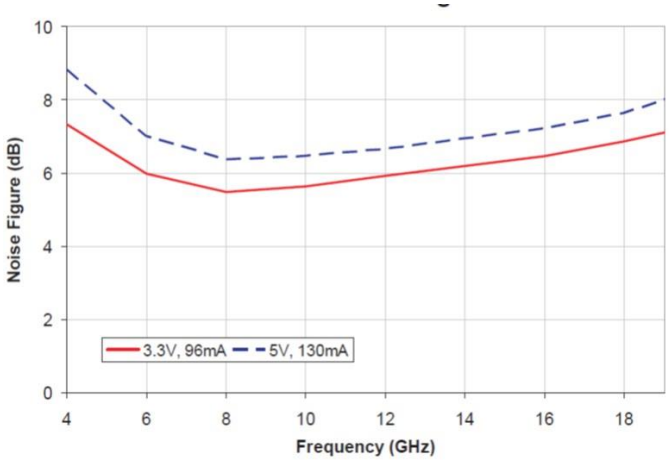
Output Power



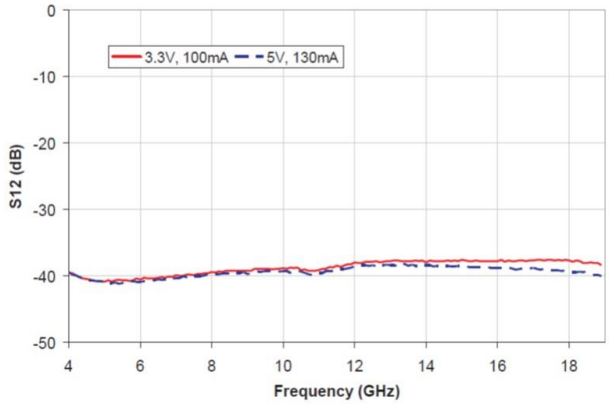
S11, S22



Noise Figure



S12



Group Delay

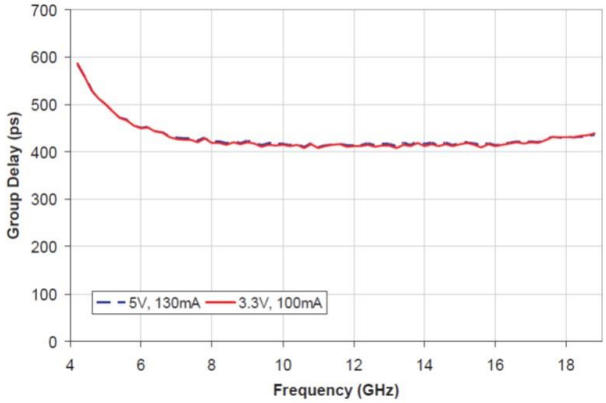


Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vd1	Drain Bias Voltage FET1	-	3.3V, 5V	6V
Id1	Drain Bias Current FET1	-	-	90mA
Vd2	Drain Bias Voltage FET1	-	3.3V, 5V	6V
Id2	Drain Bias Current FET1	-	-	110mA
Vgg1	Drain Bias Current FET1	-4	N/C	+1V
Vgg2	Drain Bias Current FET1	-4	N/C	+1V
P_{in}	Input Power (CW)	-	-	12dBm
P_{dc}	Power Dissipation	-	0.33W, 0.65W	-
T_{ch}	Channel Temperature	-	-	150˚C
Θ_{ch}	Thermal Resistance (T_{case}=85˚C)	-	60˚C/W	-
$T_{STORAGE}$	Storage Temperature[1]	-65˚C	-	150˚C

[1] Passed temperature cyling per JESD22-A104C, -65°C to +150°C, 250 cycles, dwells of 1 minute, 10°C/minute minimum ramp rate.

Caution, ESD Sensitive Device

Functional Block Diagram

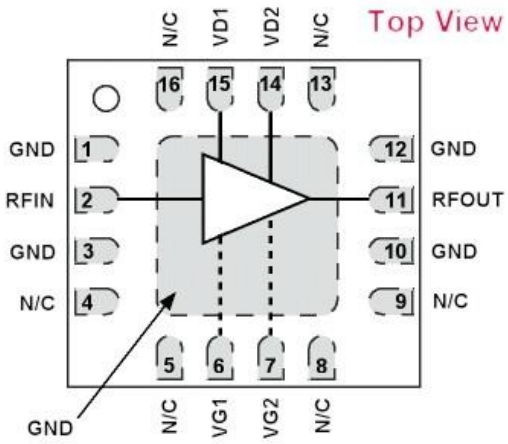


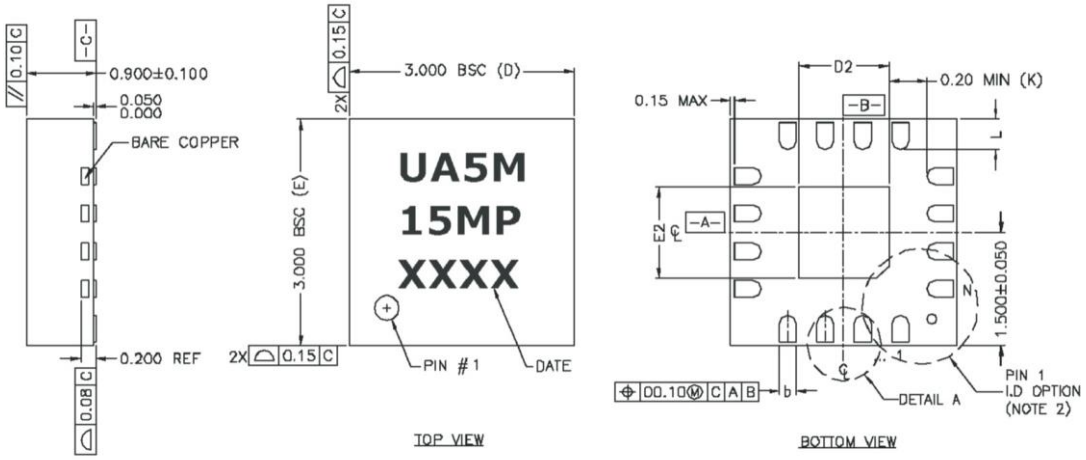
Table 2: Typical Bias Values

Vdd (V)	Idd (mA)	App
+5.0	130	Power
+4.0	110	-
+3.3	100	Gain
+2.5	79	Low-noise

Table 3: Pin Descriptions

Number	Function	Description
4, 5, 8, 9, 13, 16	N/C	No connection necessary, may be connected to DC/RF ground
1, 3, 10, 12, + paddle	GND	Must be connected to DC/RF ground
2, 11	RF IN, OUT	AC coupled and matched to 50W
6, 7	VG1, VG2	Optional 1st and 2nd gate bias lines, required > 100pF low-freq bypass capacitor if used
14, 15	VD1, VD2	1st and 2nd drain bias lines, requires>100pF low-freq bypass capacitor and clean power supply

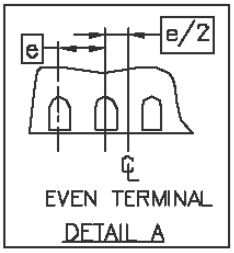
QB Package Outline



Package Notes:

- Conforms to JEDEC MO-220, revision 1
- Pin 1 ID indicated by dot on top of package
- All units millimeters, not to scale
- Pkg is 100% Pb free (lead free)
- Leadframe base is 0.2mm Cu 194 FH with Ag-ring finish
- Solder plate is 100% Sn
- All ground leads and center paddle must be connected to RF ground

VARIATION / SYMBOL	BB		
	MIN	NOM	MAX
e		0.50 BSC	
b	0.18	0.23	0.30
E2	1.60	1.70	1.80
D2	1.60	1.70	1.80
L	0.35	0.40	0.45
N		16 LD	
ND		4	
NE		4	
JEDEC VARIATION		N/A	
INTERNAL FEATURE		N/A	
PKG CODE		VQ Q16	



Lead Free (Pb-free):

The UA5M15MP QFN package contains no lead (Pb) and eliminates the need for costly re-qualification efforts, which are necessary to conform to the European mandated “Restricted use of Hazardous Substances” (RoHS) compliance.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking. PCB ground planes are not sufficient, the backside of the QFN must be soldered to the PCB, and PCB filled or plated vias must be used to conduct heat away from this contact.

ESD Handling and Bonding:

This package is ESD sensitive; preventive measures should be taken during handling and solder attach. Solder paste and flux screen printing is recommended.

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