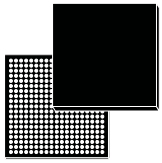
STA1080, STA1085 STA1090, STA1095

Accordo2 family - Dual core processor for car radio and display audio applications

Data brief



LFBGA361
(16x16x1.7, 0.8mm pitch)

GAPGPS00902

Features

Core and infrastructure

- ARM® Cortex™-R4 MCU
- Embedded SRAM
- SDRAM controller
- Serial QIO NOR interface executable in place
- Parallel NAND/NOR controller

Audio subsystem

- Sound processing DSPs
- Stereo channels hardware Sample Rate Converter
- Audio DACs
- Digital audio interfaces (I2S/ multichannel ports)
- Single ended stereo ADC with internal switching logic
- Differential Mono ADC with internal switching logic

Media interfaces

- Secure-Digital Multimedia Memory Card Interfaces
- USB 2.0 Interfaces
- SPDIF with CDROM block decoder support

Display subsystem

- TFT controller
- Touch Screen Controller
- Video Input Port
- Graphic acceleration

Embedded secure CAN subsystem

- Dedicated ARM Cortex-M3 core
- Isolated embedded memory
- Secured NOR interface

I/O interfaces

- General purpose ADCs
- I2C multi-master/slave interfaces
- UART Controllers
- Synchronous Serial Ports (SSP/SPI)
- GPIOs
- JTAG
- CAN ports

Operating conditions

- VDD: 1.14 V - 1.26 V
- VDDIO: 3.3 V ±10%
- VDDIOON: 3.3 V ±10%,
- Ambient temperature range: -40 / +85 °C

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1 Description

Accordo2 is a family of devices that provide a cost effective microprocessor solution for modern automotive car radio systems, with an embedded powerful Digital Sound Processing subsystem, as well as a MIPS efficient ARM Cortex-R4 processor.

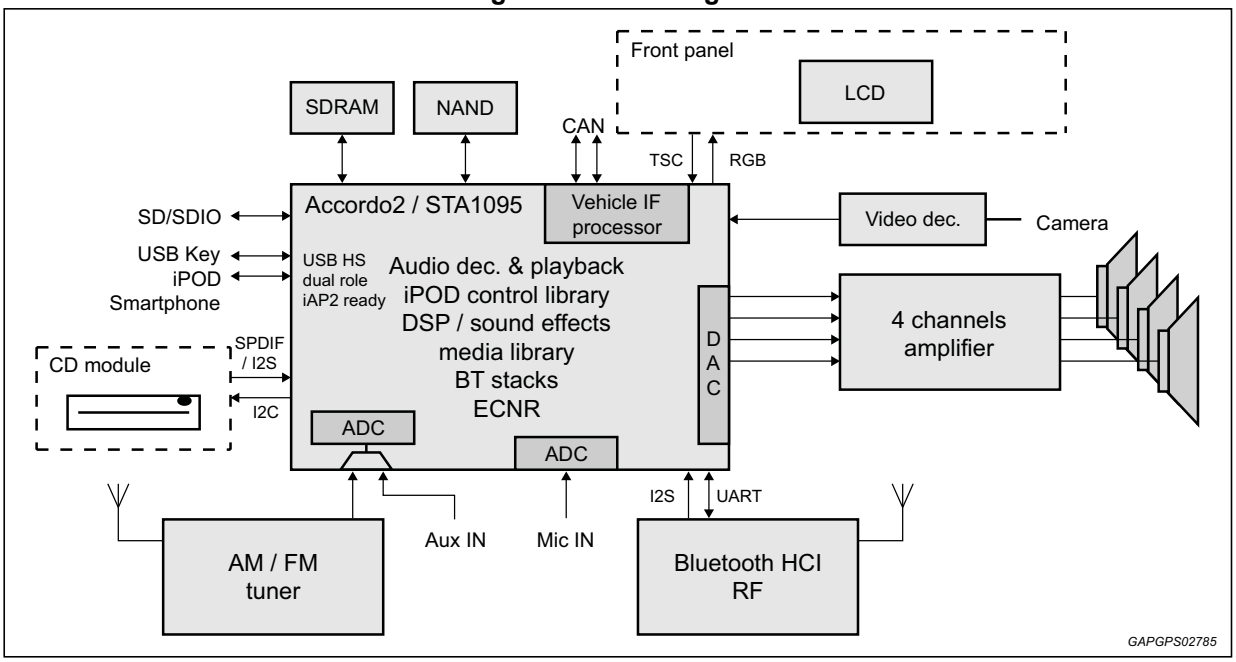
In addition, an ARM Cortex-M3 controller is dedicated for real-time CAN / Vehicle Interface Processing.

In terms of peripherals, Accordo2 family devices come with an exhaustive set of common interfaces (UART/I2S/I2C/USB/MMC) which make the device optimal for implementing a feature rich system as well as a cost effective solution.

The solution is bundled with a complete software package, which allows a very fast system implementation.

Accordo2 family devices manage the entire audio chain from analog or digital inputs to analog or digital outputs, including digital audio media decoding, sample rate conversion among various sources, intelligent routing and audio effects / DSP post processing. With its flexible memory configuration, it allows implementing from very low cost systems based on real time OS, scaling up to demanding applications based on Linux OS.

Figure 1. Block diagram



2 System description

2.1 Processor MCU

Accordo2 family devices processing capability relies on an ARM Cortex-R4. The MCU has instruction cache and data cache, as well as TCM Memory dedicated respectively to instructions and data for high throughput and low latency tasks.

2.2 Memory controller

2.2.1 Embedded memory

Accordo2 family devices embed SRAM memory, which can be used for data or code storage.

Embedded memory can be used in conjunction with executable in place NOR devices to implement cost effective solutions. The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 SDRAM controller

SDRAM controller supports SDRAM JEDEC interface 16 bits wide, which allows interfacing to automotive SDRAM memory devices to handle high footprint applications.

Such memory is cacheable, and can be accessed by DMA.

2.2.3 SQI executable in place

The SQIO controller allows interfacing Serial Quad I/O flash memories.

2.2.4 Parallel memory interface

FSMC static memory controller, provides a generic parallel interface suitable to connect to NOR devices as well as SRAM and NAND devices. This peripheral allows execution in-place from NOR/SRAMs, as well as DMA accesses.

NOR memory space can be partitioned so to reserve a portion of the parallel NOR device to the Secure CAN Subsystem.

2.3 USB

Accordo2 family devices have one USB HS interface with embedded PHY, allowing to efficiently connect to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, Accordo2 family fully support USB charger specification.

2.4 Sound subsystem

Accordo2 family devices implement a sound subsystem which allows to efficiently handle sound processing tasks, such as spatialization and equalizer, without loading the main CPU with interrupt intensive tasks.

2.4.1 Audio interfaces

A complete set of audio interfaces is provided, in order to simplify integration with amplifiers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- Audio ADC
  - Shared between AUX LINE and TUNER LINE
  - ADC Inputs are single ended 3.3 V
- Voice ADC
  - Shared among Voice and TEL-IN lines with embedded multiplexer
  - Both Mic and Tel-In lines are differential inputs
- Stereo DAC
- Multiple I2S IN
- Multiple I2S OUT
- SPDIF IN for CD/CDROM input with Hardware Block Decoder for CDROM error correction.

2.4.2 Routing and sample rate converters

Each audio interface can be routed in both directions (IN/OUT) through hardware sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as Bluetooth® Hands Free and audio media playback, to be handled without CPU load.

2.4.3 Sound DSP

Accordo2 family devices are equipped with multiple DSPs dedicated to sound processing, fully integrated with the sound subsystem with a specific isochronous bus. DSP is provided with an integrated sound processing library implementing effects like spatialization, balancing and equalizer, etc..

2.5 SDMMC

Accordo2 family devices are equipped with SDMMC controllers, which allow interfacing to either mass storage devices, or to Wi-Fi modules.

2.6 DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides independent channels which can be dynamically assigned to different data-path. Complex Scatter/gather transfers can be implemented by programming specific DMA command linked lists.

2.7 Secure CAN subsystem

Accordo2 family devices allow isolating critical code from main application by implementing a dedicated subsystem based on ARM Cortex-M3, along with:

256 KB dedicated embedded SRAM

- Dedicated embedded SRAM
- CAN controller
- Dedicated GPIOs

In order to guarantee security of CAN network, it can be completely isolated from the rest of the system, in such a way that no application running on Cortex-R4 can access by any mean to CAN specific resources. The secure sub-system communicates with the application running on Cortex-R4 using a Hardware Mailbox interrupt based mechanism.

A specific set of peripherals can be reserved and locked to be only accessible from CortexM3, thus allowing a complete independent subsystem. In addition to that, specific secure GPIOs as well as wake signals are reserved to such system.

2.8 General purpose ADC

Accordo2 family devices have general purpose ADCs with a resolution of 10-bits.

2.9 GPIOs

Accordo2 family devices have GPIOs which can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals.

2.10 Generic interfaces

2.10.1 UARTS

- Programmable baud rates up to3Mbps
- Hardware Flow control
- DMA capability

2.10.2 I^2Cs

- Master/slave modes in multi-master environment
- Multiple baud rates supported: 100/400/1000/3400 Kbits/s
- DMA capability

2.10.3 SSP/SPI ports supporting

- Motorola SPI-compatible interface
- Texas Instrument synchronous serial interface
- National Semiconductor MICROWIRE® interface
- Unidirectional interface
  - DMA capability

2.11 Video input port (VIP)

The Video Input Port (VIP) allows to grab images from external devices, supporting parallel interface up to 54 MHz. Both embedded synchronization and external synchronization are supported. VIP supports either interlaced or progressive mode.

The VIP is synchronized with display controller to prevent from tearing effects, and is used in conjunction with SGA to implement on the fly YUV->RGB color conversion and bilinear interpolated re-scaling.

2.12 Smart graphics accelerator (SGA)

The aim of the Smart Graphic Accelerator (SGA) is to provide an efficient 2D and 3D primitive drawing tool that breaks down the MIPS and power consumption concerns of pixel processing.

It supports:

- Control and synchronization features
- 2D-graphic features
- Video overlay features
- 3D graphic features

2.13 Display controller

The main features of the LCD Controller are:

- Supports single and dual panel monochrome and color STN displays up to 8 bits interfaces
- Supports single and dual panel color STN displays with 8 bits interfaces
- Supports TFT, AD-TFT and HR-TFT color displays
- Resolution programmable up to 1024 lines of 1024 pixels
- 12-bpp (4:4:4), 15+I bpp (I:5:5:5) or 16 bpp (5:6:5) true-color
- 24-bpp packed and non-packed true-color (non-palettized)
- Color enhancement (16-bpp to 18-bpp conversion) for addressing 18-bit (RGB 666) TFTpanels using only 16-bpp resolution

2.14 Touch screen controller

The Touch Screen Controller is enhanced with a movement tracking algorithm, 128 depth buffer and a programmable active window feature.

Main features are :

- Integrated 4 wire touchscreen controller
- 8 analog input, 10-bit resolution ADC

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

3.1 LFBGA361 (16x16x1.7 mm) package information

Figure 2. LFBGA361 (16x16x1.7 mm) package outline

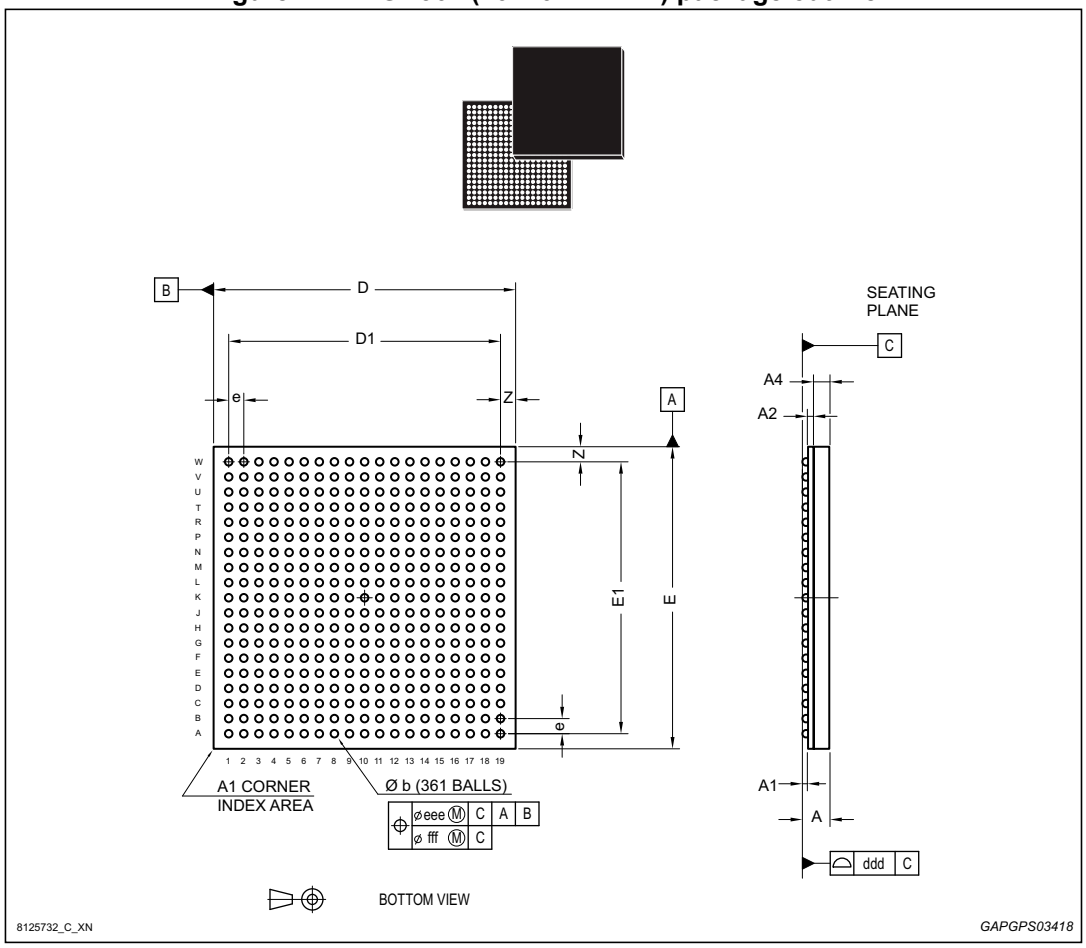


Table 1. LFBGA361 (16x16x1.7 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.7	-	-	0.0669
A1	0.25	-	-	0.0098	-	-
A2	-	0.3	-	-	0.0118	-
A4	-	-	0.8	-	-	0.0315
b	0.35	0.4	0.48	0.0138	0.0157	0.0189
D	15.85	16	16.15	0.624	0.6299	0.6358
D1	-	14.4	-	-	0.5669	-
E	15.85	16	16.15	0.624	0.6299	0.6358
E1	-	14.4	-	-	0.5669	-
e	-	0.8	-	-	0.0315	-
Z	-	0.8	-	-	0.0315	-
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

4 Order codes

Table 2. Device differentiating features

	STA1080	STA1085	STA1090	STA1095
CAN	No	Yes	No	Yes
Video Input Port	No	No	Yes	Yes
Smart Graphic Interface	No	No	Yes	Yes
Touch Screen Controller	No	No	Yes	Yes

Table 3. Ordering information

[Root] Root Code	**[Freq]** CortexR4 Frequency	**[Sec]** Security	**[Grade]** Qualification Grade	**[Pack]** Packing
1095 **1090** **1085** **1080**	**E** = *Eco (450MHz)*	**L** = *Locked*	**A** = *Automotive*	[empty] = Tray
	H = *High (533MHz)*	**O** = *Open*	**C** = *Consumer*	**TR** = *Tape&Reel*
	P = *Premium (600MHz)*			
Part number example: **STA1080EOA**				
1080	**E** = Eco (450MHz)	**O** = Open	**A** = Automotive	[empty] = Tray

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
28-Aug-2015	1	Initial release.